ABSTRACT
This paper presents the design of two stages Low-Noise Amplifier (LNA) with current reuse technique for multi-standard wireless applications. The LNA is aimed to support the requirements of the standards of GSM, WCDMA, Bluetooth, WLAN, etc., of bandwidth range of 0.5 – 3.0MHz. The target specifications include a peak power gain ($S_{21}$) of greater than 15 dB with a noise figure (NF) of less than 2 dB. The input matching ($S_{11}$) and output matching ($S_{22}$) are kept well below -15 dB while the reverse isolation ($S_{12}$) is less than -40 dB. The LNA aims at an IIP$3$ of – 4 dBm. The LNA consumes a very little power of less than 10mW while operating at 1V power supply. The circuit is designed in 90nm CMOS technology and its various performance parameters are analyzed by simulating using ADS 2008 simulator.

KEY WORDS Bluetooth, GSM, Noise Figure, Power Gain, WLAN, WCDMA

INTRODUCTION
Nowadays, due to ever increasing demand for simultaneous global roaming and all-in-one wireless phones, much research is focused in the development of multi standard transceivers was fostered. The user’s needs are becoming more crucial and ever demanding, especially in the field of wireless communication. They no more feel sufficient to use the mobile phone for voice communication, but also look forward to high date rate and multimedia communications. Due to this fact, new wireless standards evolve in order to meet such user’s requirements and set stringent requirements for RF transceivers and its components. The fourth generation of wireless telecom systems will require low power multi standard chipsets, capable of operating over a number of different communication protocols, signal conditions, etc. The efficient implementation of these chipsets calls for reconfigurable building blocks that can adopt for different specifications with minimal power consumption and at a low cost.

A typical RF receiver front-end suitable for multi standard applications is shown in Figure 1. It consists of a RF Filter, Low Noise Amplifier (LNA), followed by a down-conversion mixer, of which the LNA is of greater significance. The design of LNA is critical due to its position at the receiver front end, having to simultaneously match the antenna and to amplify weak input signals with minimal noise contribution, high linearity and isolation from the rest of receiver chain.
In multi standard receiver front end, LNA must operate over different frequency ranges, while maintaining a reduced number of passive components, i.e. capacitors and inductors to increase the integration. The ultimate use of the LNA is to amplify the weak signal received from the antenna to acceptable levels while trying to cut out the additional self generated noise. A common issue in most reported multi-standard LNAs is the need for additional passive components for input and output matching networks.

The LNA can be used in different topologies such as distributed amplifier topology, differential amplifier topology, resistive shunt feedback topology, common source (CS) topology, common gate (CG) topology. The distributed amplifier provides better input matching but it consumes large power and area. The CS amplifier provides high gain, better noise figure and better reverse isolation.

The CS amplifier adopts a band pass filter to provide good input matching and shows better performance throughout the wideband with small amount of power consumption. But, the reactive elements used in the filter networks occupy more area. This paper is presented using CG and CS topology.

During the past few years, wireless local area networks (WLAN) have been deployed all over the world as office and home communication infrastructures, where LNAs are important components in these systems. Price and other market requirements force RF receivers to be integrated in standard CMOS technology along with the rest of digital signal processing units. Integrating large amount of circuits for sure requires low power consumption design techniques; therefore wide attention has been paid to the low power fully integrated LNA designs. Several works have been reported on the
current reuse techniques in LNAs. A current reuse technique adopts a series inter-stage resonance to enhance the gain. But, using a three transistor in cascode form decreases the output swing which is not suitable for low voltage technology and introduces additional noise. Extremely low current consumption is required in short-range sensor applications where autonomous operation of several years is desired. In a sensor radio, the RF circuits are usually in the dominant role when it comes to the current consumption.

To achieve sufficient receiver performance, both the low-noise amplifier (LNA) and local oscillator (LO) signal generation circuits require remarkably more current compared to analog base band (BB). The current consumption of the RF parts is approximately 90% of the total receiver current consumption. For that reason, power optimization should be concentrated on the blocks and elements operating at the RF. The same dc current is re-used in both blocks, thus reducing the total power consumption.

In a receiver chain, LNA is usually the first active signal-processing block after the antenna. Despite all the favourable features of the systems, serious challenges still exist for the realization of receiver front-end circuits, especially for the low-noise amplifier (LNA). The received signal exhibits very low power-spectral density (PSD) at the receiver antenna, resulting in a received signal power that is typically three orders of magnitude smaller than that of the narrow-band transmission systems. The amplitude of the received signal at the input of LNA may vary from few $nV$ (less than -130dBm for GPS signals) to tens of $mV$ (e.g., large interferers accompanying the signal). The LNA should be capable of amplifying all these signals without causing any significant distortion.

The sensitivity of LNA determines the sensitivity of the overall receiver. This requires that very little noise from the LNA be introduced to the entire receiver. Another major requirement of the LNA is to provide a large gain to suppress the noise of subsequent blocks.

LNAs are usually preceded and followed by passive filters for out-of-band rejections and channel selection. The transfer function of such filters is usually a function of their termination impedance. This imposes the requirement of certain input and output impedances, such as $50\Omega$, on the LNA. On the other hand, the amount of noise introduced by the LNA is also a function of source impedance. The optimum source impedance, which results in the minimum noise figure of the LNA, may not be equal to that required by the preceding stage, e.g., $50\Omega$. This may result in an LNA having a good input matching and a poor noise figure or vice versa.
Low power consumption is also desired for the LNA and the linearity of an amplifier is traditionally described in terms of 1-dB compression point (P1 dB) and third-order intercept point (IP3). The IP3 could be an important figure-of-merit of the LNA due to the existence of strong narrow-band interferers such as the 802.11a WLAN signals in the 5- to 6-GHz band.

Figure 2: Proposed LNA

Figure 3(a) : First Stage Equivalent Circuit
CIRCUIT DESCRIPTION

The proposed LNA is designed to fulfill the requirements of a multi-standard wireless receiver for the following standards: GSM, WCDMA, Bluetooth, and WLAN. The proposed LNA is shown in Fig. 2. It consists of two stages, first stage is cascade amplifier and second stage is cascode amplifier with current reuse technique. Its equivalent circuit is also presented in Fig. 3 for both stages.

The common gate input stage is used to achieve the input matching. The input impedance of 50 Ω is matched by proper selection of device dimension and bias current. A cascode stage is used to reduce the effect of parasitic capacitance at the drain terminal of the transistors. The input impedance is given by equation (1).

\[ Z_{in} = \frac{1}{C_{gs}L_{s}} \quad \text{……}(1) \]

The first and second stage gain equation is given in (2) & (3).

\[ Gain(AV1) \approx \frac{Z_2}{Z_2 + rds_4} \times \frac{Z_1}{Z_1 + rds_1} \quad \text{……}(2) \]

\[ Gain(AV2) \approx \frac{Z_4}{Z_4 + rds_4} \times gm_3Z_3 \quad \text{……}(3) \]

where,

\[ Z_1 = (SLS_2 + SLg_2 + \frac{1}{SC_{gs}2} + \frac{1}{SC_{g}2})// \frac{1}{SC_{gd}2} \]

\[ Z_2 = Ld_2 // CGd_2 \]

\[ Z_3 = (SLS_4 + SLg_4 + \frac{1}{SC_{gs}4} + \frac{1}{SC_{g}4})// rds_3 \]

\[ Z_4 = Ld_4 // CGd_4 \]

In this proposed LNA, a current reused topology of a two-stage amplifier is adopted to share the operating current. The current-reuse technique increases the gain and reduces power consumption. On chip inductance \( L_3 \) is used for the first stage inductive load. A choice of inductive load has another advantage which is no extra dc voltage drop. The current-reused configuration can be considered as a two stage cascade amplifier, where the first stage is the CG amplifier \( M_1 \), and the second stage is cascode amplifier which
eliminates Miller effect and provides a better isolation from the output return signal. The impedance of $L_{Di}$ should be large enough provide a high impedance path to block the signal. The current-reused stage includes the transistors, the inductor, and the capacitors. The purpose of using this is to create a low impedance path without any dc current, while the impedance of increases with frequency leading to a high impedance path to block the signal. As a consequence, the input signal can be amplified twice under this con-current structure. With this design technique, a high gain can be obtained under low dc power consumption. Note that a large $C_g$ is preferred in the design for a better signal coupling. With M1 and M2 sharing the same bias current, the total power consumption of the current-reused amplifier is minimized. To achieve higher gain than a conventional cascade LNA, both M1 and M2 are in common-gate configurations. The design considerations of the current-reused LNA are similar to those of a cascaded amplifier.

![Figure 4: Power Gain (S_{21})](image1)

![Figure 5(a): Noise Figure (NF) – GSM](image2)
SIMULATION RESULTS
The proposed LNA is simulated using 90nm CMOS technology in ADS 2008 simulator. In this section the simulation results are presented in figures starting from 4 to 8. Figure 4 represents the gain for all standards. The power gain is maintained more than 10 dB for all standards at their corresponding frequency range. Figure 5(a) and 5(b) shows the noise figure (NF) characteristic of GSM and WCDMA which is achieved less than 2.5dB and Figure 5(c) shows the noise figure (NF) characteristic of WLAN which is achieved less than 3.8dB in their corresponding frequency ranges. The overall minimum value of NF is 1.9dB, obtained at 1.84GHz, which correspond to the lowest limit of the GSM band.

The figure 6, shows the input matching ($S_{11}$) of less than -10 dB for all standards at their frequency ranges. The output matching ($S_{22}$) is of -20 dB for WLAN and kept below -10 dB through out the bandwidth for all standards as shown in figure 7. The reverse gain ($S_{12}$) is falls below -82 dB over the bandwidth for all standards as shown in figure 8.
Figure 6: Input Matching ($S_{11}$)

Figure 7: Output Matching ($S_{22}$)

Figure 8: Reverse Isolation ($S_{12}$)
The stability factor characteristic of the LNA is shown in figure 9. This factor should be greater than unity to claim the circuit unconditionally stable which is attained. From the figure it is found that it is greater than unity in all the standards. The linearity of the LNA has been also taken into account in the design procedure. As shown in figure 10, the value of IIP_3 is achieved at -4dBm for WCDMA. With the current-reused technique between the two stages, the amplifier achieves a maximum power gain of 25 dB under a supply voltage of 1 V and a power consumption of only 7.458 for GSM standard, 7.86 for WCDMA standard and 7.968mW for WLAN. The table-I summarizes the performance of LNA in all three standards. The table-II presents the comparison of our LNA with recently reported ones.
Table I – Simulated Performance Summary of LNA.

<table>
<thead>
<tr>
<th>Standard</th>
<th>Gain (dB)</th>
<th>NF (dB)</th>
<th>$S_{11}$</th>
<th>$S_{22}$</th>
<th>IIP$_3$ (dBm)</th>
<th>Power (mW)</th>
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</thead>
<tbody>
<tr>
<td>GSM (1.85-1.99)</td>
<td>&gt; 12</td>
<td>&lt; 2.2</td>
<td>&lt; -10</td>
<td>&lt; -13</td>
<td>-</td>
<td>7.458</td>
</tr>
<tr>
<td>WCDMA (1.92-2.17)</td>
<td>&gt; 15</td>
<td>&lt; 2.6</td>
<td>&lt; -10</td>
<td>&lt; -11</td>
<td>-4</td>
<td>7.860</td>
</tr>
<tr>
<td>WLAN (2.4-2.4835)</td>
<td>&gt; 18</td>
<td>&lt; 3.8</td>
<td>&lt; -10</td>
<td>&lt; -20</td>
<td>-20</td>
<td>7.968</td>
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Table II – Comparison with Recently Reported Multi-Standard CMOS LNAs.

<table>
<thead>
<tr>
<th>Ref</th>
<th>Standard</th>
<th>Gain (dB)</th>
<th>NF (dB)</th>
<th>IIP$_3$ (dBm)</th>
<th>Power (mW)</th>
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<tr>
<td>[1]</td>
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<td>1.61</td>
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<td></td>
<td>WCDMA</td>
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</table>

CONCLUSION

A two stage cascaded LNA is designed using 90nm CMOS technology and simulated. Simulation results are presented and compared. A power gain of more than 10dB is achieved with a noise figure (NF) of less than 3.8dB over the bandwidth. The input matching ($S_{11}$) and output matching ($S_{22}$) are kept well below -10dB and -11dB respectively while the reverse isolation ($S_{12}$) is less than -85dB.

The LNA ensures better linearity by achieving an in band IIP$_3$ of -4dBm. The LNA consumes a very little power of less than 7.968mW while operating at 1V power supply. Thus the proposed LNA claims a low power design with low noise figure while achieving all other parameters at acceptable level over the bandwidth of 1.8 – 2.5 GHz.
REFERENCES


