A 3.1 – 4.8GHZ LOW POWER DIFFERENTIAL LNA FOR MB-OFDM ULTRA WIDEBAND APPLICATIONS

Vaithianathan. V\textsuperscript{1}, Dr. Raja. J\textsuperscript{2}, and Arun. V\textsuperscript{3}

Address for correspondence
1Dept. of ECE, SSN College of Engineering, Kalavakkam, Tamilnadu
3Dept. of IT, SSN College of Engineering, Kalavakkam, Tamilnadu
2Dept.of ECE, Anna University, Thiruchirapalli, Tamilnadu.
vaithianathanv@ssn.edu.in, rajajanakiraman@gmail.com, arunindian01@gmail.com

ABSTRACT
In this paper, a gain controllable Shunt-Series peaking differential Low Noise Amplifier (LNA) is proposed with common gate core stage and common drain buffer as an output stage. The proposed circuit is designed using 90nm CMOS technology to achieve the target specifications which include a power gain ($S_{21}$) of 10dB with a noise figure (NF) of less than 4dB over the first 3 bands of MB-OFDM and an in-band IIP\textsuperscript{3} of -1dBm. The input matching ($S_{11}$) and output matching ($S_{22}$) are kept well below -10dB while the reverse isolation ($S_{12}$) is less than -30dB. The LNA consumes a very little power of less than 12mW while operating at 1V power supply.

KEY WORDS Noise Figure, Power Gain, Shunt-Series Peaking, IIP\textsuperscript{3}

INTRODUCTION
Even though the UWB technology has been around for past three decades, there is an increased interest among researchers in recent times because of its multipath immunity and low power spectral density. Recently, great interests have been taken in developing the needed ultra-wide-band (UWB) LNAs in 3.1-10.6 GHz UWB system for wireless personal area network (WPAN) applications.

In 2002, the Federal Communications Committee (FCC) defined as UWB any signal with a fractional bandwidth larger than 20 percent at all times of transmission or occupying more than 500-MHz frequency spectrum with an average power spectral density limit of – 41.3dBm/MHz or 75nW/MHz, in the 3.1–10.6-GHz range [1]. The fractional bandwidth is defined as the ratio of bandwidth to centre frequency as given in equation (1).

$$ B_f = \frac{BW}{f_{center}} 100\% = \frac{f_h - f_l}{(f_h + f_l)/2} 100\% \quad ... (1) $$

where $f_h$ and $f_l$ are highest and lowest cut-off frequencies at the –10 dB point of a UWB pulse spectrum, respectively. This unlicensed band is intended to enable several applications such as ground penetrating radars, imaging and surveillance systems, safety/health monitoring, and wireless home video data links.

Table I: Power Consumption in HG & LG Modes

<table>
<thead>
<tr>
<th>freq</th>
<th>I_DC.</th>
<th>..._Lowgain..IDC.i</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0000Hz</td>
<td>12.00 mA</td>
<td>11.09 mA</td>
</tr>
</tbody>
</table>
There are two types of UWB Communication systems based on direct sequence CDMA (DS-CDMA) approach and multi-band orthogonal frequency division multiplexing (MB-OFDM) approach. From the literature it is understood that DS-CDMA approach also called impulse radio employs short duration pulses to provide data rates from 28 to 1320 Mb/s within the transmission bands from 3.1 to 4.85 GHz and from 6.2 to 9.7 GHz. In the MB-OFDM approach, the 3.1–10.6-GHz band is divided in 14 channels organized in five groups and the operation within the first group is mandatory, while all the other groups are optional. This is illustrated in Figure 1.

A typical MB-OFDM front-end consists of a Low Noise Amplifier (LNA), Low Pass Filter (LPF), Mixer and Variable Gain Amplifier (VGA) is shown in Figure 2. The design of LNA plays crucial role since it determines overall system performance.

![Figure 1: MB-OFDM UWB Spectrum](image1)

![Figure 2: A typical MB-OFDM UWB Front End](image2)
Table-II: Simulation Results Summary and Performance Analysis

<table>
<thead>
<tr>
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<th></th>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>90nm CMOS</td>
<td>0.13um CMOS</td>
<td>0.18um CMOS</td>
<td>90nm CMOS</td>
<td>90nm CMOS</td>
</tr>
<tr>
<td>BW (GHz)</td>
<td>0.1 – 4</td>
<td>2 – 4.6</td>
<td>3.1 – 4.8</td>
<td>3.1 – 4.8</td>
<td>3.1 – 4.8</td>
</tr>
<tr>
<td>Gain S_{21}(dB)</td>
<td>12.1</td>
<td>9.5</td>
<td>10 – 16</td>
<td>9.2 – 10.3</td>
<td>9.8– 10.9</td>
</tr>
<tr>
<td>NF (dB)</td>
<td>8.4</td>
<td>3.5</td>
<td>3 – 4</td>
<td>3.8 – 4.06</td>
<td>2.38 – 2.64</td>
</tr>
<tr>
<td>IIP3 (dBm)</td>
<td>-12.83</td>
<td>-0.8</td>
<td>-5.1</td>
<td>&lt; - 1</td>
<td>&lt; - 1</td>
</tr>
<tr>
<td>Input Matching S_{11} dB</td>
<td>&lt; - 10</td>
<td>&lt; - 10</td>
<td>&lt; - 10</td>
<td>&lt; - 13</td>
<td>&lt; - 10</td>
</tr>
<tr>
<td>Reverse Gain S_{12}(dB)</td>
<td></td>
<td></td>
<td></td>
<td>&lt; -33</td>
<td>&lt; -30</td>
</tr>
<tr>
<td>Output Matching</td>
<td>&lt; - 10</td>
<td>&lt; - 10</td>
<td>&lt; - 10</td>
<td>&lt; - 10.4</td>
<td>&lt; - 10.6</td>
</tr>
<tr>
<td>S_{22} (dB)</td>
<td>&lt; - 10</td>
<td>&lt; - 10</td>
<td>&lt; - 10</td>
<td>&lt; - 11.09</td>
<td>&lt; 12</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>10.2</td>
<td>16.5</td>
<td>32.4</td>
<td>&lt; 11.09</td>
<td>&lt; 12</td>
</tr>
</tbody>
</table>

The design of an LNA involves numerous trade-offs such as power gain, noise figure, input and output matching, reverse gain and input third order intercept point (IIP3). The amplifier must have sufficient gain to overcome mixer noise contribution, but not so much common mode signal to cause mixer overload. The LNA should also be linear one for a wide range of input signal powers and should consume very low power [2].

The LNA can be used in different topologies such as distributed amplifier topology, differential amplifier topology, Shunt-Series peaking feedback topology, common source (CS) topology, and common gate (CG) topology. With the advances of CMOS technology and availability of accurate CMOS device and passive element models, many CMOS distributed amplifiers having relatively flat gains over very wide bands within the dc to 40-GHz with better input matching. But the major drawback of distributed amplifiers for UWB applications is their large dc power consumption, severely limiting their usage in wireless portable devices. This is due to the fact that several parallel transistors, with each transistor draining current from the source, are needed to form the required artificial transmission lines and to achieve a reasonable gain on a 50- load [3].
Figure 3: Proposed Gain Controllable Shunt-Series peaking CG Differential LNA

Figure 4: Equivalent Circuit (for one section only)
The Shunt-Series feedback amplifier provides wideband matching and flat gain but it suffers with poor noise figure and large power consumption. The CS amplifier provides high gain, better noise figure and better reverse isolation but it uses a filter network to provide wideband input matching which occupies more area. The differential LNA is preferred over other topologies as it offers better immunity to environmental noise, improved linearity, low power consumption. Firstly, the virtual ground formed at the ‘tail’ removes the sensitivity to parasitic ground inductances. Secondly the differential amplification of the signal ensures attenuation of the common mode signal, in most systems this common mode signal will be noise. Thirdly, the use of mixers and image rejection schemes require to be fed from a differential source. So, in our proposed design differential amplifier topology with Shunt-Series peaking is used to achieve wide bandwidth, flat gain as well as low noise figure. Section II discusses the operation of the proposed low power current reuse gain controllable Shunt-Series peaking CG differential LNA. This section also explains the operation of a gain controlling circuit to operate LNA in high gain and low gain modes. The current reuse technique used for reducing the power consumption is also explained. In Section III, the simulation results with performance analysis are presented. The results are compared in both the high gain and low gain modes and also with the recently published works.

Figure 5: Gain Controlling Circuit

CIRCUIT DESCRIPTION

The proposed low power current gain controllable resistive Shunt-Series peaking common gate differential amplifier is shown in Figure 3. Its equivalent circuit is also presented in Figure 4. The transistor M₁ (M₄) provides the low frequency power gain along with wideband input matching. When the parasitic capacitance is also considered, the input impedance of the proposed circuit is given by the equation (2)

\[ Z_{IN} \approx \frac{sL_{s1}}{1 + (g_{m1} + sC_{gs1})sL_{s1}} \]  \hspace{1cm} (2)

The parasitic capacitance present in the equation (2) will make the input matching get worse at a high frequency. In order to obtain best input matching, an inductor \( L_{S1} \) must be added at the input node to resonate with the parasitic capacitance. The best input matching is obtained at the resonant frequency given by the equation (3)

\[ \omega_r \approx \frac{1}{\sqrt{C_{gs1}L_{S1}}} \]  \hspace{1cm} (3)

The resonant frequency is fixed at the centre of our band of interest by suitably selecting the values of \( C_{gs1} \) and \( L_{S1} \). The source degeneration inductors (\( L_{S1} \) and \( L_{S2} \)) in Shunt-Series with the parasitic capacitances \( C_{gs1} \) and \( C_{gs2} \) are used to ensure better input matching without degrading the noise figure and power gain except at lower UWB. Thus, the input matching of 50Ω can be easily achieved.

The transistor M₃ (M₄) used as another CG stage provides high frequency power gain and is also used to reduce the effect of the parasitic capacitance at drain terminal of M₁ (M₄). This provides better reverse isolation (\( S_{12} \)) with the sufficient gain, higher bandwidth. The proposed circuit uses a Balun network (balanced-unbalanced) to perform single-ended to differential conversion at the input and vice versa at the output. A variety of bandwidth enhancement techniques such as Shunt-Series peaking, Shunt-Series peaking, T-coil and \( f_T \) doubler are commonly used. In the proposed LNA, the Shunt-Series peaking load is used to achieve the bandwidth of 1.7GHz in the range 3.1 to 4.8GHz. By choosing the optimum values of \( L_1 \) (\( L_2 \)) and \( R_1 \) (\( R_2 \)), a good flatness over the frequency band of interest is achieved.

The common drain amplifier has low output impedance thereby enabling easy output matching of 50Ω. The output impedance can be easily matched by using equation (4).

\[ R_{out} \approx r_{d3} \]  \hspace{1cm} (4)

This buffer is simply a source follower with a current source IB₅. The circuit is biased by exact selection of component values and transistor dimensions.

The proposed LNA can be made to work in two modes as high gain mode and low gain mode with the help of controlling switches \( S_1 \) and \( S_2 \) as shown in Figure 5. The high gain operation is achieved with the closed switch \( S_1 \) and open switch \( S_2 \). The low gain operation is...
achieved with the open switch $S_1$ and closed switch $S_2$. The low power consumption has a high priority especially for mobile applications. Nowadays a competitive value for power consumption is less than 15mW.

In this paper, a two-stage common gate (CG) amplifier is adopted to share the operating current to achieve lower power consumption with the help of LD$_1$ and CD$_1$. The first stage is the CG amplifier $M_1$ ($M_2$), and the second stage of another CG amplifier $M_3$ ($M_4$) which provides a better reverse isolation from the output return signal, also a Common Drain (CD) $M_5$ ($M_6$) is used for Output impedance matching in the third stage. The purpose of using CD$_1$ is to create a low impedance path without any dc current, while the impedance of LD$_1$ increases with frequency leading to a high impedance path to block the signal. For Bandwidth enhancement the combined Shunt-Series Peaked of $R_1$ ($R_2$), $L_1$ ($L_2$), and $L_3$ ($L_4$) are employed. As a consequence, the input signal can be amplified twice under this concurrent structure. With this design technique, a high gain can be obtained under low dc power consumption. Since we have adopted a CG stages, the achieved gain is in the range of 9 – 11dB with the power consumption as low as 12mW.

![Figure 6: Power Gain (S$_{21}$)](image-url)
SIMULATION RESULT
The proposed LNA is simulated using 90nm CMOS technology in ADS 2008 simulator. In this section, the simulations results for high gain mode and low gain mode are presented in figures starting from 6 to 11. From the Figure 6, one can see that in high gain mode, a maximum of 17dB is achieved at 3.9GHz while more than 12dB is maintained from 3.1GHz to 4.8GHz. The Figure 6 also reveals that in low gain mode, a maximum of 16dB is achieved at 3.8GHz while more than 11dB is maintained in the entire bandwidth. In the high gain mode, the achieved noise figure falls in the range of 0.25dB to 1.45dB while achieving a minimum of 0.25dB at 3.8GHz. In the low gain mode, the achieved noise figure falls less than 1.45dB while a minimum of 1.1dB is achieved at 3.8GHz.
In both modes of operation the noise figure is maintained with very small variations throughout our band of interest, which is the major achievement of the proposed LNA. These results are illustrated in Figures 7(a) and 7(b).

![Figure 7(a): Noise Figure (NF) in HG Mode](image1)

![Figure 7(b): Noise Figure (NF) in LG Mode](image2)
The input matching \((S_{11})\) is kept well below \(-10\)dB and \(-13\)dB in high gain mode and low gain mode respectively. The output matching \((S_{22})\) is kept well below \(-10.4\)dB to \(-10.6\)dB in both the modes of operation as shown in Figures 8 and 9. In high gain mode, the reverse gain falls below \(-33\)dB while it falls below \(-30\)dB in the low gain mode. This ensures the better stability for the circuit. These results are plotted in Figure 10.

The stability factor, ‘\(K\)’ is calculated over the frequency band 3 - 5GHz by using the equation (5). The value of “\(K\)” is greater than 1 and hence the circuit is unconditionally stable.

\[
K = \frac{1 + |S_{p22} - S_{p21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2 |S_{p21}|} \ldots \ldots (5)
\]

A two tone test is used to measure the IIP\(_3\). In both modes of operation, the LNA ensures better linearity by achieving IIP\(_3\) of \(-1\)dBm as shown in Figure 11.

The proposed LNA consumes 11.09mW in low gain mode and 12mW in high gain mode while operating at 1V power supply which is illustrated in table – I. Thus, the current-reuse technique is used to increase the gain and reduce power consumption.

The table – II summarizes the results achieved by the proposed LNA by simulating in 90nm CMOS technology using Agilent’s ADS 2008 simulator. From the table, we can claim that our proposed LNA performs better as compared with other LNAs.

![Figure 8: Input Matching (S\(_{11}\))](image-url)
Figure 9: Output Matching ($S_{22}$)

Figure 10: Reverse Isolation ($S_{12}$)

Figure 11: Input 3rd Order Intercept Point (IIP₃)
CONCLUSION
A gain controllable Shunt-Series peaking feedback differential LNA is designed using 90nm CMOS technology and simulated. The LNA is operated in high gain and low gain modes by using gain controlling switches. The results obtained in both the modes are presented and compared. An average power gain of 11dB is achieved with a noise figure (NF) of 2.64dB over the first 3 bands of MB-OFDM and an in-band IIP3 of -1dBm. The input matching (S11) and output matching (S22) are kept well below -12dB while the reverse isolation (S12) is less than -40dB. The LNA ensures better linearity by achieving an IIP3 of –1dBm. The LNA consumes a very little power of less than 6.251mW while operating at 1V power supply. Thus the proposed LNA claims a low power design while achieving all other parameters at acceptable level.

REFERENCES