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Review Article

DIFFERENT TYPES OF MULTILEVEL INVERTER TOPOLOGIES – A TECHNICAL REVIEW

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ABSTRACT:

This paper presents a review and analysis of multilevel inverter topologies. Multilevel inverters are most widely used for medium-voltage high-power converter like fans, pumps and material transport drives. In this active area, different inverter topologies, circuits, advantages and drawbacks are discussed. Multilevel Inverter topologies such as diode-clamped, flying-capacitor, cascaded H-bridge, hybrid H-bridge, new hybrid H-bridge and new cascaded multilevel inverter have been discussed in the literature. In this work a new idea is developed to increase the level with less number of switches. It is concluded that the topologies are closely related to each particular application, depending on their unique features and limitations like power or voltage level, performance, reliability, costs and other technical specifications.

I .INTRODUCTION

Numerous industrial applications have began to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and MW power level. For a medium voltage grid, it is troublesome to connect one power semiconductor switch directly. The application of ac variable frequency speed regulations are widely popularized , high power and medium voltage inverter has recently become a research focus so far as known there are many problems in conventional two level inverter in the high power application. Multilevel inverter have been gained more attention for high power application in recent years which can operate at high switching frequencies while producing lower order harmonic components[1]-[6],

A multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel inverter system for a high power application [7] - [12]. There are several topologies such as neutral point clamped inverter, flying capacitor based multilevel, cascaded H-bridge multilevel inverter, hybrid H-bridge multilevel inverter and new hybrid H-bridge multilevel inverter [13]-[15]. Figure 1 shoes the various multilevel inverter topologies.

This paper discusses the operation of different topologies for multilevel inverter which can produce multilevel; under this condition neutral point clamped multilevel inverter is presented, which has a simple structure and good performance .This topology effectively reduce the higher input dc voltage that each device must withstand. The main disadvantage still exists in this topology, which restricts the use of it to the high power range of operation [16]-[20].

The first topology introduced is the series H-bridge design [21]-[22], from this several configurations have been obtained. This topology consists of series power conversion cells which form the cascaded H-bridge multilevel inverter and power levels may be scaled easily. An apparent disadvantage of this topology is the large number of isolated voltage required to supply each cell. By using H-bridge power conversion cells several topologies are developed and their advantages and disadvantages are discussed.

The proposed topology for multilevel inverter has a high number of steps associated with a low number of power switches. In addition for producing all levels at the output voltage, a procedure for calculating the required dc voltage source is proposed.

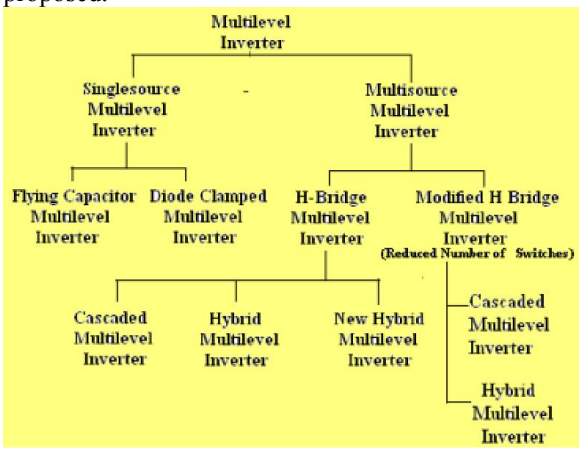

Figure 1.Types of Multilevel Inverter Topologies

II.DIODE- CLAMPED MULTI LEVEL INVERTER:

A three-phase six-level diode-clamped inverter is shown in figure.2. Each of the three phases of the inverter shares a common dc bus, which has been subdivided by five capacitors into six levels. The voltage across each capacitor is V_{dc} and the voltage stress across each switching device is limited to V_{dc} through the clamping diodes. This involves the (n-1) main dc-link capacitors and also Σ (2n-2) clamping diodes, where n-number of levels. For DCMLI requires a large number of clamping devices as 2n-2. . Each phase has five complementary switch pairs such that turning on, one of the switches of the pair require that the other complementary switch be turned off. The complementary switch pairs for phase leg **a** are (Sa1, Sa'1), (Sa2, Sa'2), (Sa3, Sa'3), (Sa4, Sa'4), and (Sa5, Sa'5). The figure.3 shows the line voltage waveform of a fifteen-level diode clamped multilevel inverter. The main advantages are the entire phases share a common dc bus, which minimizes the capacitance requirements of the converter. For this reason, a back-to-back topology is not possible and can be practically used for a high-voltage back-to-back inter-connection or an adjustable speed drive. The capacitors can be pre-charged as a group and efficiency is high for fundamental frequency switching. The main draw backs are real power flow is difficult for a single inverter because the intermediate dc levels will tend to overcharge or discharge without precise monitoring and control. The number of clamping diodes required is quadratically related to the number

of levels, which can be cumbersome for units with a high number of levels [23]-[30].

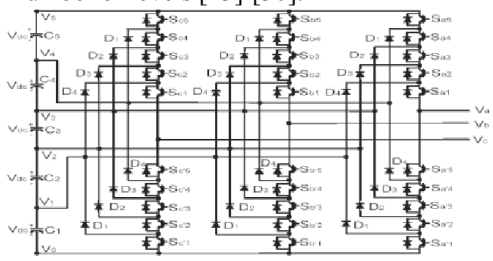

Figure 2. Three phase diode-clamped multilevel inverter

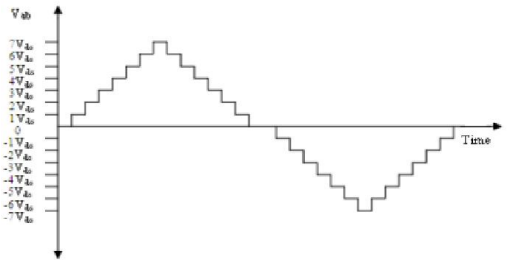

Figure 3. Line voltage waveform of diode-clamped multilevel inverter

III.FLYING CAPACITOR BASED MULTILEVEL INVERTER:

The FCMLI requires a large number of capacitors to clamp the device (switch) voltage to one capacitor voltage level provided all the capacitors are of equal value, an n-level inverter will require a total number of (n-1)(n-2)/2 clamping capacitors per phase leg in addition to (n-1) main dc bus capacitors. Figure.4 shows the three phase six level flying capacitor based multilevel inverter. Let us consider the group of capacitors in a single clamping leg as one equivalent capacitor, which is also applicable for 'n' level inverter. If the voltage of the main dc –link capacitor is V_{dc}, the voltage of inner most capacitor, the inner most two devices is $V_{dc}/ (n-1)$. The voltage of the inner most capacitor will be $V_{dc}/ (n-1) + V_{dc}/ (n-1) = 2V_{dc}/ (n-1)$ and so on. Each next clamping capacitor will have the voltage increment of $V_{dc}/ (n-1)$ from its immediate inner one voltage levels. The arrangements of the flying capacitors in the FCMLI structure assures that the voltage stress across each main device is same and is equal to $V_{dc}/ (n-1)$ for an 'n' level inverter. The advantages of this topology are phase redundancies are available for balancing the voltage levels of the capacitors, real and reactive power flow controlled.

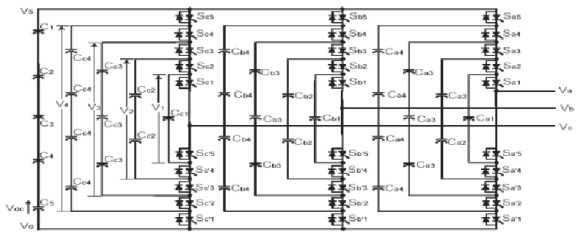

Figure 4. Three phase Flying Capacitor based Multilevel Inverter

The large number of capacitors enables the inverter to ride through short duration outages and deep voltage sags. The main draw back of this topology is complicated to track the voltage levels for all of the capacitors. Also the pre charging of all the capacitors to the same voltage level and startup are complex. Switching utilization and efficiency are poor for real power transmission. The large numbers of capacitors are more expensive and bulky than clamping diodes in multilevel diode-clamped converters. Packaging is also difficult in inverters with a high number of levels [31] - [40]. The figure.5 shows the line voltage waveform of a fifteen-level diode clamped multilevel inverter.

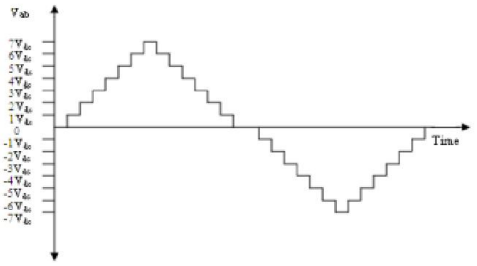

Figure 5. Line voltage waveform of flying capacitor based multilevel inverter

IV.CASCADED H-BRIDGE MULTILEVEL INVERTER:

The general structure of the cascaded multilevel inverter for single phase is shown in figure 6. Each of the separate voltage source (V_{dc1}, V_{dc2}, V_{dc3}) connected in cascade with other sources via a special H-bridge circuit associated with it. Each of the circuit consists of four active switching elements that can make the output voltage source in positive or negative polarity; or it can be simply zero volts depending on the switching condition of the switches in the circuit. A conventional multilevel power inverter topology employs multiple/link voltage of equal magnitudes. It is fairly easy to generalize the number of distinct levels. [41]- [55]

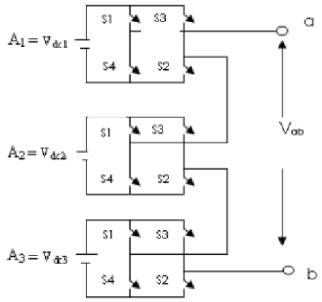

Figure 6.Topology for Cascaded H-Bridge Multilevel Inverter

The S number of dc source or stages and the associated number output level can be calculated by using the equation

$N_{level} = 2S+1$ (1)

For example if S=3, the output wave form has 7 levels (±3, ±2, ±1 and 0)

The voltage on each stage can be calculated by using the equation,

$A_i = 1V_{dc}$ (i=1,2,3……) (2)

The number of switches used in this topology is given by the equation,

$N_{switch} = 4S$ (3)

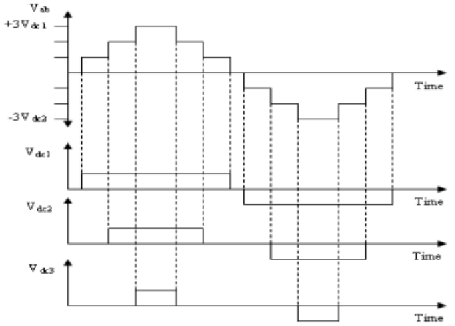

Figure 7. Typical Output Waveform for Cascaded H-Bridge Multilevel Inverter

The advantages of the cascaded multilevel inverter are series H-bridges for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and cheaply. The draw back of this topology needs a separate dc source for each of the H-bridges. This will limit its application in products that already have multiple SDCSs [56]-[72]. Figure 7 shows the output voltage waveform of a 7-level cascade inverter with 3 separate dc sources.

V. HYBRID H-BRIDGE MULTILEVEL INVERTER:

The general structure of the hybrid multilevel inverter is in figure 8. Each of the separate voltage source (S_1, S_2,) connected in cascaded with other sources via a special H-bridge circuit associated with it. Each of the circuit consists of four active switching elements that can make the output voltage source in positive or in negative polarity; or it can be simply zero volts depending on the switching condition of the switches in the circuit. The main advantages of hybrid multilevel inverter are high number of levels with reduced number of bridges and dc sources. [73]-[83]. The S number of dc source or stages and the associated number output level can be calculated by using the equation

$$N_{level} = 2^{S+1} - 1 \quad (4)$$

For example if S=3, the output wave form has 7 levels (±3, ±2, ±1 and 0) which is shown in the figure 9 and voltage across the capacitor (S) on each stage can be calculated by using the equation

$$A_i = 2^{S-1}.V_{dc} \quad (i=1, 2\ldots n) \quad (5)$$

The number of switches used in this topology is given by the equation

$$N_{switch} = 4S \quad (6)$$

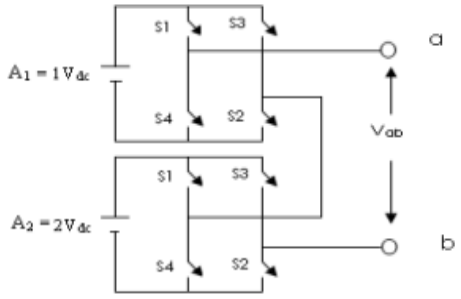

Figure 8. Topology of Hybrid H-Bridge Multilevel Inverter

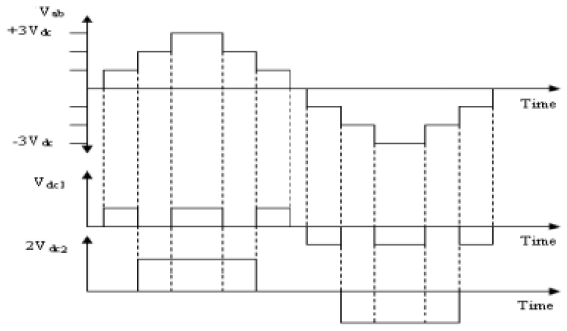

Figure 9. Typical Output Voltage Waveform for Hybrid H-Bridge Multilevel Inverter

VI.NEW HYBRID H-BRIDGE MULTILEVEL INVERTER:

The general structure of the new hybrid multilevel inverter is in figure 10, each of the separate voltage source (V_1, V_2, V_3) connected in cascaded with other sources via a special H-bridge circuit associated with it. Each of the circuit consists of four active switching elements that can make the output voltage source in positive or negative polarity; or it can be simply zero volts depending on the switching condition of the switches in the circuit. The main advantages of hybrid multilevel inverter are high number of levels with reduced number of bridges and dc sources [84]-[92]. The S number of dc source or stages and the associated number output level can be calculated by using the equation

$$N_{level} = 3^S \quad (7)$$

For example s=3, the output wave form has 27 levels (±13, ±12, ±11, ±10, ±9, ±8, ±7, ±6, ±5, ±4, ±3, ±2, ±1 and 0) which is shown in the figure 11 and voltage on each stage (S) can be calculated by using the equation

$$A_i = 3^{S-1}.V_{dc} \quad (i=1, 2\ldots n) \quad (8)$$

The number switches used in this topology is given by the equation

$$N_{switch} = 4S \quad (9)$$

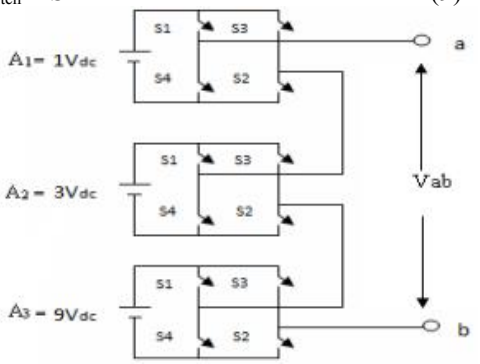

Figure 10. Topology for New Hybrid H-Bridge Multilevel Inverter

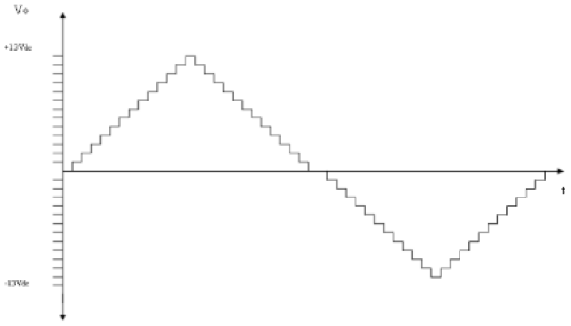

Figure 11. Typical output waveform for New Hybrid H-Bridge Multilevel Inverter

VII. CASCADED MULTILEVEL INVERTER WITH REDUCED NUMBER OF SWITCHES:

The proposed topology for multilevel inverter with a high number of steps associated with a low number of power switches for producing all levels (odd and even) at the output voltage, a procedure for calculating the required dc voltage source is proposed. This unit requires bidirectional switches with the capability of blocking voltage and conducting current in both the directions. The advantages of this configuration over the previous one is that each bidirectional switch requires or gate driver circuit therefore this configuration is widely used in multilevel inverter [93]-[94].

For wide range of steps this unit can be connected in series as shown in the figure 12. The number of switches and steps associated with this topology is given by the following equation

$$N_{switch} = n_1 + n_2 + \ldots\ldots n_k \quad (10)$$

$$N_{step} = n_1 \times n_2 \times \ldots\ldots \times n_k \quad (11)$$

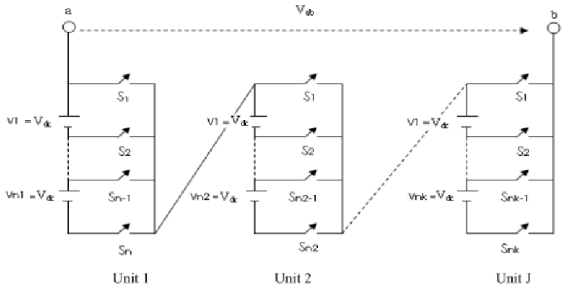

Figure 12. Topology for cascaded multilevel inverter with reduced number of switches

For symmetrical configuration of each unit the above equation becomes

$N_{switch}=n \times k$ (12)

$N_{step}=n^{k}$ (13)

From the equation (9) and (10) we get number of steps in terms of number of switch given by

$N_{step}=n^{(Nstep/2}$ (14)

The dc voltage on each unit is given by

Unit 1: $V_1=V_{dc}$ (15)

Unit2: $V_2 = (n_1\text{-}1)\, V_1+V_1=n_1V_{dc}$ (16)

Unit3: $V_3= (n_1\text{-}1)\, V_1+ (n_2\text{-}1)\, V_1+V_1=n_1\, n_2\, V_{dc}$ (17)

Similarly dc voltage source on j^{th} unit can be calculated as follows

$V_k = V_1 + (n_i\text{-}1)\, V_i =n_i . V_{dc}$ (i=1,2….k-1) (18)

The figure .13 gives only the positive output voltages only. It is shown in the waveform

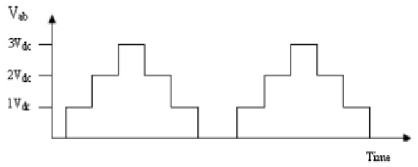

Figure 13. Output waveform only positive direction

To get both (positive and negative) half cycle one H-bridge is added with the load side it clearly shown in the figure 14.The switches Q1and Q2 are fired together and conduct for $0 < t < T$. At $t = T$, The switches Q1 and Q2 are turned off and the switches Q3 and Q4 are turned on. Thus, Q3 and Q4 conduct for the duration $T < t<2T$. For this duration, the direction of V_L is opposite to V_o, the negative half of the output wave is obtained.

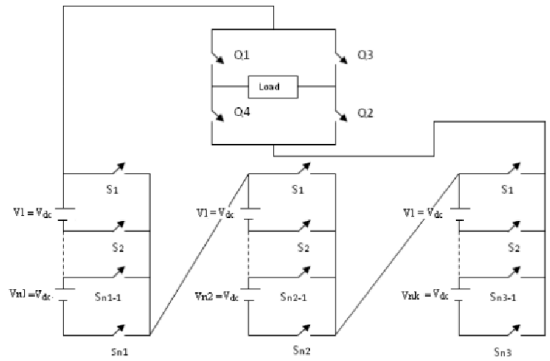

Figure 14. Circuit diagram for cascaded multilevel inverter with reduced number of switches

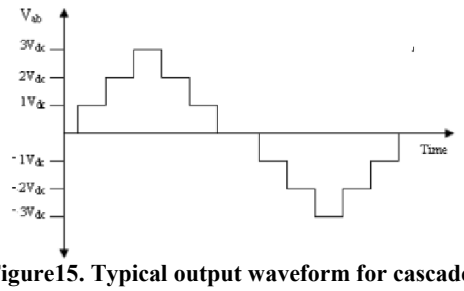

Figure15. Typical output waveform for cascaded multilevel inverter with reduced number of switches

It is clear that both switches Q1 and Q4 (orQ2 and Q3) cannot be ON simultaneously because a short circuit across the voltage V_O would be produced. The figure 15 shows the corresponding output waveform.

VIII. HYBRID MULTILEVEL INVERTER WITH REDUCED NUMBER OF SWITCHES:

The proposed method multilevel inverter has general structure of the hybrid multilevel inverter is in figure 16.Each of the separate voltage source (V_{s1}, V_{s2}, V_{s3}) connected in cascade with other sources via a special circuit associated with it. Each stage of the circuit consists of only two active switching elements that can make the output voltage source only in positive polarity with several levels; or it can be simply zero volts depending on the switching condition of the switches in the circuit. Only one H-bridge is connected to get both positive and negative polarity. The main advantages of this hybrid multilevel inverter are high number of levels with reduced number of bridges and dc sources [95]- [100] The S number of dc source or stages and the associated number output level can be calculated by using the equation

$N_{level} =2^{S+1}\text{-}1$ (19)

For example if S=3, the output wave form has 15 levels (±7, ±6, ±5, ±4, ±3, ±2, ±1 and 0) which is shown in the figure 17 and voltage on each stage can be calculated by using the equation

$A_i=2^{S-1}.V_{dc}$ (i=1, 2, 3…) (20)

The number switches used in this topology is given by the equation

$N_{switch}=2S +4$ (21)

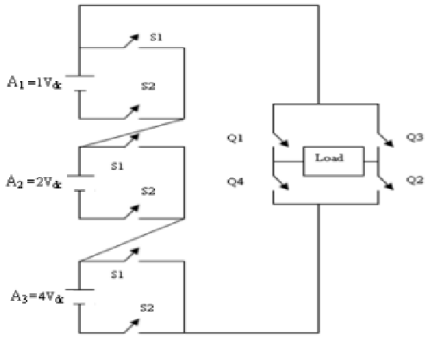

Figure 16. Topology of Hybrid Multilevel Inverter with reduced number of switches

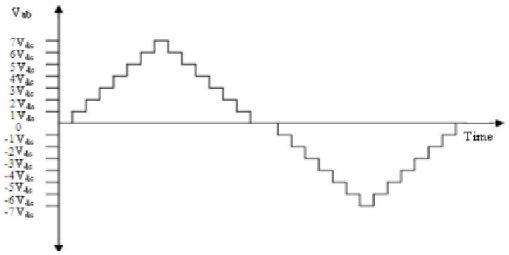

Figure 17. Line voltage waveform of Hybrid Multilevel Inverter with reduced number of switches

IX. MODIFIED HYBRID MULTILEVEL INVERTER WITH REDUCED NUMBER OF SWITCHES:

The proposed method multilevel inverter has a general structure of the hybrid multilevel inverter is shown in figure 18. Each of the separate voltage source (V_{dc1}, V_{dc2}, V_{dc3}) connected in cascade with other sources via a special circuit associated with it. Each stage of the circuit consists of only one active switching element and one bypass diode that can make the output voltage source only in positive polarity with several levels. The basic operation is to

turn on S1 (S2 and S3 turn off) and the output voltage is $+1V_S$, turning on S2 (S1 and S3 turn off) producing output $+2V_S$. Similarly other step can be achieved by turning on the suitable switches at particular intervals, table.1 shows the operation clearly. Only one H-bridge is connected to get both positive and negative polarity. The main advantage of modified hybrid multilevel inverter is high number of levels with reduced number of stages and dc sources. The S number of dc source or stages and the associated number output level can be calculated by using the equation

$$N_{level} = 2^{S+1} - 1 \quad (22)$$

For example if S=3, the output wave form has 15 levels (±7, ±6, ±5, ±4, ±3, ±2, ±1 and 0) which is shown in the figure 19, and voltage on each stage can be calculated by using the equation

$$A_i = 2^{S-1}.V_{dc} \quad (i=1, 2, 3\ldots) \quad (23)$$

The number switches used in this topology is given by the equation

$$N_{switch} = S + 4 \quad (24)$$

Table 1: basic operation of hybrid multilevel inverter

s.no	Intervals	On switches	Off switches	Voltage levels	Current flow path
1	I	S1	S2 , S3	+1Vs	S1,D2,D3
2	II	S2	S1 , S3	+2Vs	S2,D1,D3
3	III	S1,S2	S3	+3Vs	S1,S2,D3
4	IV	S3	S1 , S2	+4Vs	D1,D2,S3
5	V	S1,S3	S2	+5Vs	S1,D2,S3
6	VI	S2,S3	S1	+6Vs	D1,S2,S3
7	VII	S1,S2,S3	-	+7Vs	S1,S2,S3
8	VIII	-	S1, S2 , S3	0	D1,D2,D3

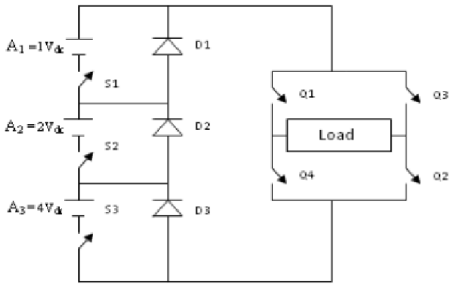

Figure 18. Topology for Modified Hybrid Multilevel Inverter

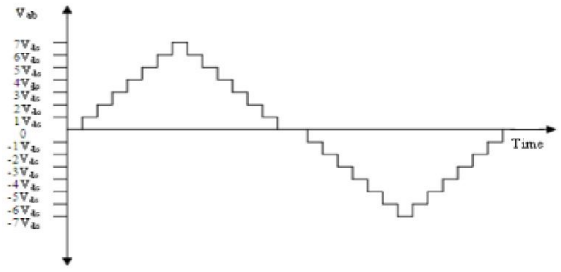

Figure 19. Line voltage waveform of Modified for Hybrid Multilevel Inverter

X. COMPARISON OF MULTILEVEL INVERTERS

The various topologies of multilevel inverters are compared according to the levels associated with the number of switches used. The graph drawn based on between the number of switches used versus types of topology for both single source and multisource multilevel inverter. From figure 20 the single source multilevel inverters has the ten switches to achieve six level for both DCMLI and FCMLI. In FCMLI there are fifteen number of capacitors and no diodes are used, but in the DCMLI five main capacitors with eight diodes. The modified hybrid multilevel inverter has advantages of fifteen level with only seven number of switches while multisource used. From figure 21 shows the modified hybrid multilevel inverter has advantages of fifteen level with only seven number of switches while multisource used. The tabulation shows the various topologies associated with its number voltage source used, number of switches and voltage levels at each topologies.

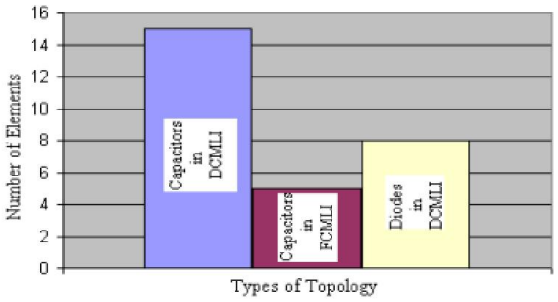

Figure 20. Comparison of single source multilevel inverters

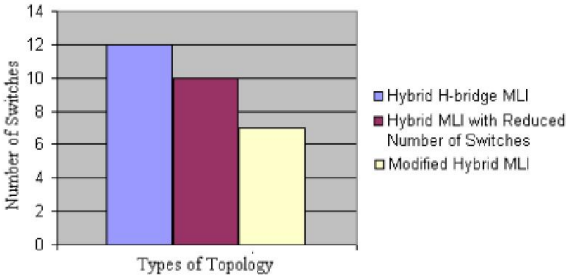

Figure 21. Comparison of multisource multilevel inverters

Table 2: comparison of multilevel inverters

S.NO	Name of the Topology	Voltage level on each stage(S)	Number of output level	Number of switches used
1	Diode clamped MLI	Vs-on each 'C'	N_C +1(No of 'C')	N_C
2	Flying capacitor MLI	SV_{dc}/ (n-1)	S	S-1
3	Cascaded MLI	$S\,V_{dc}$	S	4S
4	Hybrid MLI	$2^{S-1}.V_{dc}$	2^{S+1} -1	4S
5	New hybrid MLI	$3^{S-1}.V_{dc}$	3^{S+1} -1	4S
6	New cascaded MLI	SV_{dc}	S	2S+4
7	Hybrid MLI with reduced number of switches	$2^{S-1}.V_{dc}$	2^{S+1} -1	2S+4
8	Modified Hybrid MLI	$2^{S-1}.V_{dc}$	2^{S+1} -1	S+4

XI.CONCLUSION

This paper has demonstrated the state of the art of multilevel inverter topology. Fundamental multilevel inverter structures and its basic operations have been discussed. A procedure for calculating the required voltage level on each stage has been described. In the conventional methods as the number of levels are increased the required number of switches also increased. Due to involvement of high number of switches thereby increasing the harmonics, switches losses, cost and the total harmonics distortion the proposed method dramatically reduces the switches for high number of levels. Which will reduce the switching losses, cost and low order harmonics, effectively improves Total harmonics distortion. The possible future enlargements of multilevel inverter topologies are proposed.

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